**WHAT IS CLAIMED IS:**

1. A data processor comprising:

an instruction execution pipeline comprising N processing stages capable of executing a load instruction;

a status register capable of storing a modifiable configuration value, said modifiable configuration value having a first value indicating said data processor is capable of executing a misaligned access handling routine and a second value indicating said data processor is not capable of executing a misaligned access handling routine;

a misalignment detection circuit capable of determining if said load instruction performs a misaligned access to a target address of said load instruction and, in response to a determination that said load instruction does perform a misaligned access, generating a misalignment flag; and

exception control circuitry capable of detecting said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value.

2. The data processor as set forth in Claim 1 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execute said misaligned access handling routine.

3. The data processor as set forth in Claim 2 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said second value, determines if said load instruction is speculative.

4. The data processor as set forth in Claim 3 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

5. The data processor as set forth in Claim 4 further comprising a data protection unit capable of determining if said load instruction accesses a restricted area of memory.

6. The data processor as set forth in Claim 5 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, causes said data processor to execute an exception handling routine.

7. The data processor as set forth in Claim 6 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, is further capable of determining if said load instruction is speculative.

8. The data processor as set forth in Claim 7 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

9. A processing system comprising:

a data processor;

a memory coupled to said data processor;

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, said data processor comprising:

an instruction execution pipeline comprising N processing stages capable of executing a load instruction;

a status register capable of storing a modifiable configuration value, said modifiable configuration value having a first value indicating said data processor is capable of executing a misaligned access handling routine and a second value indicating said data processor is not capable of executing a misaligned access handling routine;

a misalignment detection circuit capable of determining if said load instruction performs a misaligned access to a target address of said load instruction and, in response to a determination that said load instruction does perform a misaligned access, generating a misalignment flag; and

exception control circuitry capable of detecting

said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value.

10. The processing system as set forth in Claim 9 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execute said misaligned access handling routine.

11. The processing system as set forth in Claim 10 wherein said exception control circuitry, in response to a determination that said modifiable configuration value is equal to said second value, determines if said load instruction is speculative.

12. The processing system as set forth in Claim 11 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

13. The processing system as set forth in Claim 12 further comprising a data protection unit capable of determining if said load instruction accesses a restricted area of memory.

14. The processing system as set forth in Claim 13 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, causes said data processor to execute an exception handling routine.

15. The processing system as set forth in Claim 14 wherein said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, is further capable of determining if said load instruction is speculative.

16. The processing system as set forth in Claim 15 wherein said exception control circuitry, in response to a determination that said load instruction is speculative, causes said data processor to dismiss said load instruction.

17. For use in a data processor comprising: 1) an instruction execution pipeline comprising N processing stages capable of executing a load instruction and 2) a status register capable of storing a modifiable configuration value, the modifiable configuration value having a first value indicating the data processor is capable of executing a misaligned access handling routine and a second value indicating the data processor is not capable of executing a misaligned access handling routine, a method of handling exceptions in the data processor comprising the steps of:

determining if the load instruction is performing a misaligned access to a target address of the load instruction;

in response to a determination that the load instruction is performing a misaligned access, generating a misalignment flag;

detecting the misalignment flag and in response thereto determining if the modifiable configuration value is equal to the first value.

18. The method as set forth in Claim 17 further comprising the step of:

in response to a determination that the modifiable configuration value is equal to the first value, executing the misaligned access handling routine.

19. The method as set forth in Claim 18 further comprising the step of:

in response to a determination that the modifiable configuration value is equal to the second value, determining if the load instruction is speculative.

20. The method as set forth in Claim 19 further comprising the step of:

In response to a determination that the load instruction is speculative, causing the data processor to dismiss the load instruction.